CON C

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Anatoliy V. Tsyrganovich

Assignee: ZiLOG, Inc.

Title: "ADC With Reduced Quantization Noise and Programmable Bit Resolution"

Serial No.: 10/821,517   Filed: April 9, 2004

Patent No.: 7,068,197 B1   Issued: June 27, 2006

Atty. Doc. No.: ZIL-537-1P   Art Unit: 2819

July 3, 2006

ATTN: Certificate of Correction Branch
COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE OF CORRECTION

Pursuant to 37 CFR 1.322, Applicant requests that the Director issue a certificate of correction to correct mistakes in the printing of the above-identified patent incurred through the fault of the Patent Office. Mistakes in the printing of claim 1 are clearly apparent when the attached pages of USP 7,068,197 (marked to show the mistakes) are compared to the attached page of the Listing of Claims that was submitted on June 2, 2006, in a Rule §1.312 Amendment After Allowance. The §1.312 Amendment was made in response to the attached Examiner's amendment. Text of the requested correction is submitted on the attached page of the Certificate of Correction form, PTO/SB/44.

Respectfully submitted,

[signature]

Darien K. Wallace
Attorney for Applicant
Reg. No. 53,736
Customer No. 47,713

11 | 12

changing values, such as ambient temperature or the expansion of a span of a bridge. An example of a high-speed, low-resolution application is the determination of the precise time at which an event takes place, such as the time at which ignition occurs in an engine cylinder.

A user can program the embodiment of FIG. 14 to filter out quantization noise that is most prevalent in the upper and most ranges of digital amplitude of intermediary digital data stream 75. Where intermediary digital data stream 75 is ten bits wide, signal analysis device 36 compares the digital amplitude of various data points of intermediary digital data stream 75 to the four boundaries between five amplitude ranges. FIG. 7 illustrates the four boundaries between fifth range 61, fourth range 60, first range 55, second range 58 and third range 59, which are defined by the 10-bit reference values seven, fifteen, one thousand seven, and one thousand fifteen, respectively. The four 10-bit reference values are stored in the four·sets of amplitude reference registers 85–88. For example, the first reference value, the ten-bit value equaling seven, is stored in two of the three 8-bit amplitude reference registers 85.

Where intermediary digital data stream 75 is twenty-four bits wide, signal analysis device 36 compares the digital amplitude of various data points of intermediary digital data stream 75 to four different boundaries between five new amplitude ranges. The amplitude ranges wherein non-random quantization noise is most prevalent in intermediary digital data stream 75 can be empirically determined through testing. In one example, the boundaries of the five noise ranges of 24-bit intermediary digital data stream 75 are defined by the four 24-bit reference values equaling 131, 071, 262,143, 16,515,071 and 16,646,143. In the process of programming SDADC 28 to operate in a 24-bit mode, processor 76 writes these four 24-bit reference values into the four sets of amplitude reference registers 85–88. For example, the fourth reference value, the 24-bit value equaling 16,646,143, is stored in the three 8-bit amplitude reference registers 88.

After signal analysis device 36 compares the digital amplitude of a data point of intermediary digital data stream 75 to the four boundaries between five amplitude ranges, signal analysis device 36 supplies two-bit signal analysis code 42 to filter control device 37. Signal analysis code 42 indicates the digital amplitude range of the data point, and therefore the likely amount of quantization noise. The embodiment of SDADC 28 in FIG. 14 then lowers the cut-off frequency of variable low-pass filter 35 in the manner described for the previous embodiments when a data point of intermediary digital data stream 75 has a digital amplitude in a range of high quantization noise.

Intermediary digital data stream 75 may contain noise other than quantization noise. In addition to determining the level of quantization noise by sensing digital amplitude, the embodiment of FIG. 14 also senses the general noise level by calculating the average deviation of a predetermined number of data points of intermediary digital data stream 75. When SDADC 28, processor 76 and the other circuitry of the embodiment of FIG. 14 sense a high general noise level, multiplexer groups 93–96 of signal analysis device 36 select an alternative set of reference values that expand the amplitude ranges for which the cut-off frequency of variable low-pass filter 35 is lowered.

Successive data points of intermediary digital data stream 75 are periodically written into noise detection registers 80–82. For example, sixteen points of data are written every 1024th data point. Processor 76 then reads the data points of intermediary digital data stream 75 and

calculates the average deviation of the sixteen data points to the average value of the sixteen points. When the calculated average deviation exceeds a predetermined value, processor 76 outputs a high-noise select signal. The high-noise select signal causes each multiplexer of multiplexer groups 93–96 to select a bit from noise reference registers 89–92. In one example, the boundaries of the five noise ranges for a high level of noise of 24-bit intermediary digital data stream 75 are defined by the four alternative reference values: 262,143, 524,287, 16,252,927 and 16,515,071.

In yet another embodiment of a sigma-delta analog-to-digital converter, filter control device 37 receives a high-noise select signal from processor 76. This embodiment does not contain the four sets of three noise reference registers 89–92, and none of the amplitude ranges is expanded when a high noise level is detected. When the calculated average deviation of a predetermined number of data points of intermediary digital data stream 75 exceeds a predetermined value, the high-noise select signal causes filter control device 37 to lower the cut-off frequency of variable low-pass filter 35 by an additional predetermined amount for each range of digital amplitude.

Although the present invention has been described in connection with certain specific embodiments for instructional purposes, the present invention is not limited thereto. Modulators having different noise shaping characteristics can be used. In some cases, noise is shaped both to higher and lower frequencies that the frequency band of interest. In such cases, both the filter of the sigma-delta converter portion, as well as the filter of the post converter filter portion are band-pass filters. In one specific embodiment, for example, second frequency response curve 51 resembles the transfer function of a band-pass filter rather than a low-pass filter. In that embodiment, variable low-pass filter 35 is replaced with a variable band-pass filter. The lower tail portions of the band-pass filter realized by the variable band-pass filter are used to filter out non-random quantization noise that has a frequency lower than the frequency band 46 of analog input signal 38.

In yet another embodiment, variable low-pass filter 35 is a finite impulse response (FIR) digital filter rather than an infinite impulse response (IIR) digital filter. In yet another embodiment, digital low-pass filter 31 includes a decimation circuit that reduces the data rate of digitized input signal 38, which is output by sigma-delta modulator 30. Although the amplitude of the digital data stream is described as representing the voltage of an input signal, the amplitude in other embodiments can represent the current of an input current signal. The post converter filter portion can be controlled to vary filter attributes other than the cutoff frequency. For example, the post converter filter portion can be controlled to change the attenuation in the stop band of the filter. In yet another embodiment, variable low-pass filter 35 is switched off when the amplitude of the digital data stream is in the first range of smaller amplitude corresponding to a smaller quantization noise.

Accordingly, various modifications, adaptations, and combinations of various features of the described embodiments can be practiced without departing from the scope of the invention as set forth in the claims.

What is claimed is:

1. A circuit comprising:

a sigma-delta converter portion that outputs a digital data stream with a digital amplitude, the digital data stream being N bits wide in a first mode and M bits wide in a second mode; and

missing text of §312 amendment

a post converter filter portion that receives the digital data stream, the post converter filter portion having a cut-off frequency that is determined at least in part based on the digital amplitude of the digital data stream.

2. The circuit of claim 1, wherein the digital data stream is a series of multi-bit digital values, each multi-bit digital value having N bits in the first mode and M bits in the second mode, wherein the series of multi-bit digital values has 2^N different digital values in the first mode and 2^M different digital values in the second mode, and wherein the digital amplitude at a given point in time is one of the multi-bit digital values.

3. The circuit of claim 1, wherein in the first mode, the post converter filter portion has a first cut-off frequency when the digital amplitude of the digital data stream is in a first amplitude range, and the post converter filter portion has a second cut-off frequency when the digital amplitude of the digital data stream is in a second amplitude range.

4. The circuit of claim 3, further comprising:
a register that stores a reference value corresponding to the digital amplitude at a boundary between the first amplitude range and the second amplitude range.

5. The circuit of claim 4, further comprising:
a processor, wherein the register is writable by the processor.

6. The circuit of claim 3, wherein the sigma-delta converter portion has a digital low-pass filter having a fixed cut-off frequency, wherein the first cut-off frequency of the post converter filter portion is higher than the fixed cut-off frequency, and wherein the second cut-off frequency of the post converter filter portion is lower than the fixed cut-off frequency.

7. The circuit of claim 1, wherein the sigma-delta converter portion comprises a sigma-delta modulator and a digital low-pass filter.

8. The circuit of claim 1, wherein post converter filter portion comprises a variable low-pass filter, and wherein the variable low-pass filter is an infinite impulse response digital filter.

9. The circuit of claim 1, wherein the circuit is an integrated circuit.

10. The circuit of claim 1, wherein the post converter filter portion includes a variable low-pass filter, the variable low-pass filter being controlled by a digital filter control value, the digital filter control value being determined at least in part based on the digital amplitude of the digital data stream.

11. The circuit of claim 1, wherein the digital data stream has a noise level, and wherein the cut-off frequency of the post converter filter portion is determined at least in part based on the noise level of the digital data stream.

12. The circuit of claim 11, wherein the noise level of the digital data stream is calculated based on an average deviation of a predetermined number of the multi-bit digital values of the digital data stream.

13. The circuit of claim 1, wherein M is larger than N, and wherein the cut-off frequency in the first mode when the digital amplitude equals A is the same as the cut-off frequency in the second mode when the digital amplitude has a value that is greater than A.

14. A method, comprising:
receiving a digital data stream from a sigma-delta converter portion, the digital data stream having a digital amplitude and containing noise;
setting a cut-off frequency of a variable filter of a post converter filter portion based at least in part on the digital amplitude of the digital data stream; and
passing the digital data stream through the variable filter such that the post converter filter portion filters out a portion of the noise.

15. The method of claim 14, wherein the digital data stream is N bits wide in a first mode and M bits wide in a second mode, and wherein the cut-off frequency in the first mode when the digital amplitude equals A is the same as the cut-off frequency in the second mode when the digital amplitude equals A times M divided by N.

16. The method of claim 15, further comprising:
programming a value for N and a value for M.

17. The method of claim 14, wherein the setting the cut-off frequency comprises:
writing a reference value to a register, wherein the reference value corresponds to a boundary of an amplitude range.

18. The method of claim 14, wherein the setting the cut-off frequency comprises:
determining the digital amplitude of the digital data stream; and
comparing the digital amplitude to a boundary of an amplitude range.

19. The method of claim 14, wherein the digital data stream has a noise level, and wherein the setting the cut-off frequency is based at least in part on the noise level of the digital data stream.

20. A sigma-delta analog-to-digital converter, comprising:
a sigma-delta converter portion that outputs an intermediary digital data stream of multi-bit digital values, each of the multi-bit digital values having N bits, the intermediary digital data stream having noise; and
means for receiving the intermediary digital data stream and for outputting a digital data stream of multi-bit digital values such that the digital data stream has less noise than the intermediary digital data stream, wherein each of the multi-bit digital values of the digital data stream has N bits, and wherein the means is programmable to receive the intermediary digital data stream in a first mode for which N is a first value and in a second mode for which N is a second value.

21. The sigma-delta analog-to-digital converter of claim 20, wherein each of the intermediary digital data stream and the digital data stream has 2^N possible digital values.

22. The sigma-delta analog-to-digital converter of claim 20, wherein the means comprises:
means for analyzing a digital amplitude of the intermediary digital data stream and for outputting a filter control value; and
a variable filter that receives the filter control value from the means for analyzing.

23. The sigma-delta analog-to-digital converter of claim 20, wherein the means filters the intermediary digital data stream with a variable filter.

* * * * *

Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application.

Listing of Claims

1. (currently amended) A circuit comprising:

a sigma-delta converter portion that outputs a digital data stream with a digital amplitude, the digital data stream being N bits wide in a first mode and M bits wide in a second mode, wherein the sigma-delta converter portion includes a sigma-delta modulator and a filter; and

a post converter filter portion that receives the digital data stream, the post converter filter portion having a cut-off frequency that is determined at least in part based on the digital amplitude of the digital data stream.

2. (original) The circuit of claim 1, wherein the digital data stream is a series of multi-bit digital values, each multi-bit digital value having N bits in the first mode and M bits in the second mode, wherein the series of multi-bit digital values has $2N$ different digital values in the first mode and $2M$ different digital values in the second mode, and wherein the digital amplitude at a given point in time is one of the multi-bit digital values.

3. (original) The circuit of claim 1, wherein in the first mode, the post converter filter portion has a first cut-off frequency when the digital amplitude of the digital data stream is in a first amplitude range, and the post converter filter portion has a second cut-off frequency when the digital amplitude of the digital data stream is in a second amplitude range.

JUL 11 2006
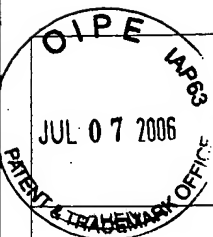
Supplemental *Notice of Allowability*	Application No. 10/821,517	Applicant(s) TSYRGANOVICH, ANATOLIY V.
	Examiner LAM T. MAI	Art Unit 2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *4/10/2006*.

2. ☐ The allowed claim(s) is/are _____.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All   b) ☐ Some*   c) ☐ None   of the:

        1. ☐ Certified copies of the priority documents have been received.

        2. ☐ Certified copies of the priority documents have been received in Application No. _____.

        3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

    * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.

    (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached

        1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.

    (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)
1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Lam T. Mai

JUL 11 2006

	Application No.	Applicant(s)
Interview Summary	10/821,517	TSYRGANOVICH, ANATOLIY V.
	Examiner	Art Unit	
	LAM T. MAI	2819	

All participants (applicant, applicant's representative, PTO personnel):

(1) *LAM T. MAI, PTO Personnel*.   (3)_____.

(2) *Jerry Wallace,Applicant's representation* .   (4)_____.

Date of Interview: *10 April 2006*.

Type: a)☒ Telephonic   b)☐ Video Conference
       c)☐ Personal [copy given to: 1)☐ applicant   2)☐ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes   e)☒ No.
   If Yes, brief description: _____.

Claim(s) discussed: *Claim 1*.

Identification of prior art discussed: *USP 6,577,258*.
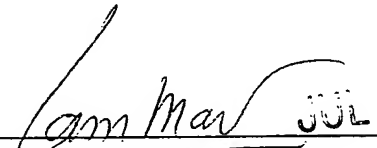
Agreement with respect to the claims f)☒ was reached.   g)☐ was not reached.   h)☐ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *ADD "wherein the sigma delta converter portion includes a sigma delta modultion and a filter" after semicolon (;) at end of line 5 (counting from beginning of claim 1)..*

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN A NON-EXTENDABLE PERIOD OF THE LONGER OF ONE MONTH OR THIRTY DAYS FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

Examiner Note: You must sign this form unless it is an Attachment to a signed Office action.

Examiner's signature, if required

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes

and/or additions be unacceptable to applicant, an amendment may be filed as provided

by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be

submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview

with Jerry Wallace, Reg. No. 53,736, (925)621-2121 on 4/10/2006.

The application has been amended as follows:

Claim 1, Line 5 (counting from beginning of claim 1), After semicolon (;) ADD

"wherein the sigma delta converter portion includes a sigma delta modulation and a

filter".

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to LAM T. MAI whose telephone number is (571)272-1807.

The examiner can normally be reached on 5:30 am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Barnie Rexford can be reached on (571) 272-7492. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300.

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

Page __1__ of __1__

PATENT NO.   : 7,068,197 B1

APPLICATION NO.: 10/821,517

ISSUE DATE   : June 27, 2006

INVENTOR(S)   : Tsyrganovich

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 12, line 67, the following text should be added after the words "in a second mode" and before the semicolon --, wherein the sigma-delta converter portion includes a sigma-delta modulator and a filter--

Thus, lines 63-68 of column 12 should read:

1. A circuit comprising:
a sigma-delta converter portion that outputs a digital data
    stream with a digital amplitude, the digital data stream
    being N bits wide in a first mode and M bits wide in a
    second mode, wherein the sigma-delta converter portion
    includes a sigma-delta modulator and a filter; and

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Darien K. Wallace, Silicon Edge Law Group LLP
6601 Koll Center Pkwy, Suite 245
Pleasanton, CA 94566

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.